REMARKS

The Applicant thanks the Examiner for the thorough examination of the application. No new matter is believed to be added to the application by this Amendment.

Status of the Claims

Claims 1, 3-16 and 19-20 are pending in the application. The claims have been amended to improve their language and to better set forth the invention being claimed.

Rejections Under 35 U.S.C. §103(a) Based On Nakano

Claims 1, 5, 11, 16, 19 and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Nakano (U.S. Patent 6,529,181). Claims 3, 4, 7-9, 12-15, 17 and 18 are rejected under 35 U.S.C. §103(a) as being obvious over Nakano in view of Uchino (U.S. Patent 6,040,816). The Examiner adds the teachings of Itakura (U.S. Patent 5,252,957) to Nakano (as applied to claim 1) to reject claims 2, 6 and 10 under 35 U.S.C. §103(a) as being obvious. Applicant traverses.

The present invention, as set forth in amended independent claim 1, recites a novel combination of elements including a feature of "a timing controller outputting to the respective source drivers at least two clock signals having different phases, the timing controller separately outputting R/G/B data synchronized with each clock signal to the source drivers", a feature of "at least two data buses transmitting the data separately output from the timing controller to the respective source drivers, respectively", and a feature of "the at least two data buses are connected between the timing controller and the respective source drivers, a number of the data

buses are in proportion to a number of clock signals output from the timing controller, and the source drivers separately sample the data to thereby reduce electricity consumption". Claim 11 similarly sets forth a method for driving an LCD device.

None of cited references teaches or suggests at least the above-mentioned features of the present invention.

In Nakano, at least two clock signals D4 and D5 are not applied to the respective source driver 130, one D4 of the at least two clock signals is applied to odd-numbered source drivers, and one D5 of the at least two clock signals is applied to even-numbered source drivers 130 (see col. 6, lines 38-43).

The fundamental differences between the present invention and Nakano can be better understood by referring to Figures 5A and 5B of Nakano, which are reproduced below.

FIG. 5A

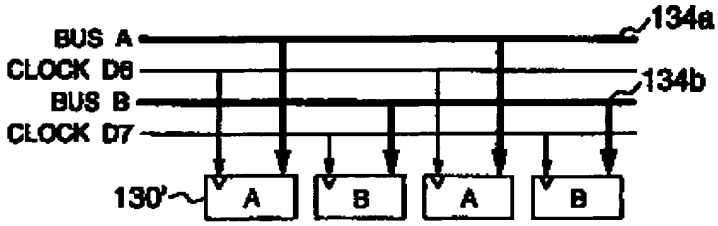
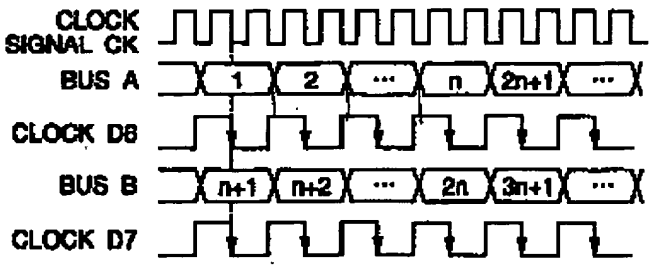


FIG. 5B



In Figures 5A and 5B of Nakano, at least two data buses do not transmit the data to the respective source drivers and are not connected between the timing controller and the respective source drivers. One bus line 134a of two data buses transmits the data to odd-numbered source drivers and is connected between the timing controller and the odd-numbered source drivers, and the other bus line 134b of two data buses transmits the data to even-numbered source drivers and is connected between the timing controller and the even-numbered source drivers.

In contrast, the present invention has "at least two data buses transmitting the data separately output from the timing controller to the respective source drivers, respectively" as is set forth in claim 1 (*see also* independent claim 11). As a result, Nakano utterly fails to disclose or suggest the source driving technology set forth in independent claims 1 and 11 of the present invention. The teachings of the secondary references fail to address these deficiencies of Nakano.

As a result, one of ordinary skill in the art would not be motivated by Nakano (alone or in combination with Uchino or Itakura) to produce claims 1 and 11 of the present invention. A *prima facie* case of obviousness has not been made. Claims depending upon claims 1 or 11 are patentable for at least the above reasons. These rejections are overcome and withdrawal thereof is respectfully requested.

Prior Art Cited But Not Utilized By The Examiner

The prior art cited but not utilized by the Examiner shows the status of the conventional art that the invention supersedes. No additional remarks are accordingly necessary.

EHC/REG/bsh

The Drawings

The Examiner has found the drawing figures to be acceptable in the Office Action mailed March 22, 2004.

Priority

The Examiner has acknowledged priority most recently in the Office Action Summary of the Office Action mailed March 22, 2004.

Assignment

The assignment was recorded on December 28, 2001 at reel 012420, frames 0478-0480.

Conclusion

The Examiner's rejections have been overcome, obviated or rendered moot. No issues remain. The Examiner is accordingly respectfully requested to place the application in condition for allowance and to issue a Notice of Allowability.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert E. Goozner (Reg. No. 42,593) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

EHC/REG/bsh

Pursuant to the provisions of 37 C.F.R. §§ 1.17 and 1.136(a), the Applicants hereby petition for an extension of two (2) months to August 10, 2006 in which to file a reply to the Office Action. The required fee of $450.00 is enclosed herewith.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Dated: August 4, 2006
REG

Respectfully submitted,

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